

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a buried insulating film formed on the  
5 semiconductor substrate;

a plurality of single crystalline semiconductor  
layers, each having a semiconductor element formed  
therein and being formed on the buried insulating film;  
and

10 an element isolation region formed between  
adjacent single crystalline semiconductor layers,  
the element isolation insulating films formed in  
the element isolation region and having substantially  
the same height from the surface of the semiconductor  
15 substrate.

2. The semiconductor device according to claim 1,  
wherein at least one of said plurality of single  
crystalline semiconductor layers differs in thickness  
from other single crystalline semiconductor layers.

20 3. The semiconductor device according to claim 1,  
wherein

the single crystalline semiconductor layers  
include

a first single crystalline semiconductor layer  
25 having a MOS transistor formed therein; and

a second single crystalline semiconductor layer  
having a bipolar transistor formed therein, said first

and second single crystalline semiconductor layers having substantially the same film thickness and a thickness of the semiconductor layer lower than the gate electrode of the MOS transistor being lower than the film thickness of the second single crystalline semiconductor layer.

4. The semiconductor device according to claim 2, wherein

the single crystalline semiconductor layers include

a first single crystalline semiconductor layer having a MOS transistor formed therein; and

a second single crystalline semiconductor layer having a bipolar transistor formed therein, said first and second single crystalline semiconductor layers having substantially the same film thickness and a thickness of the semiconductor layer lower than the gate electrode of the MOS transistor being lower than the film thickness of the second single crystalline semiconductor layer.

5. The semiconductor device according to claim 1, wherein, in the single crystalline semiconductor layers, a full depletion element and a partially Depletion element are formed.

6. The semiconductor device according to claim 2, wherein, in the single crystalline semiconductor layers, a full depletion element and a partially Depletion

element are formed.

7. The semiconductor device according to claim 3,  
wherein, in the single crystalline semiconductor layers,  
a full depletion element and a partially Depletion  
5 element are formed.

8. The semiconductor device according to claim 4,  
wherein, in the single crystalline semiconductor layers,  
a full depletion element and a partially Depletion  
element are formed.

10 9. A semiconductor device comprising:  
a semiconductor substrate having a first region  
and a second region;

a buried insulating film formed in the first  
region of the semiconductor substrate;

15 at least one first single crystalline  
semiconductor layer having a semiconductor element  
formed therein and formed in the buried insulating film  
and;

20 at least one second single crystalline  
semiconductor layer formed in the second region and in  
contact with the semiconductor substrate; and

an element isolation region for isolating the  
single crystalline semiconductor layers from each other,

25 wherein all the element isolation insulating films  
in the element isolation region have the same height  
from the semiconductor substrate.

10. The semiconductor device according to claim 9,

wherein the first single crystalline semiconductor layer formed in the first region consists of a plurality of semiconductor layers having a plurality of film thicknesses.

5           11. The semiconductor device according to claim 9, wherein a CMOS element is formed in the first region and a bipolar element is formed in the second region.

          12. The semiconductor device according to claim 10, wherein a CMOS element is formed in the first region  
10          and a bipolar element is formed in the second region.

          13. The semiconductor device according to claim 9, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a  
15          predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer  
20          lower than the gate electrode of the MOS transistor is substantially the same as the thickness of a predetermined second single crystalline semiconductor layer.

          14. The semiconductor device according to claim 10, wherein a MOS transistor is formed in a predetermined  
25          first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor

layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer lower than the gate electrode of the MOS transistor is substantially the same as the thickness of a predetermined second single crystalline semiconductor layer.

15. The semiconductor device according to claim 11, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer lower than the gate electrode of the MOS transistor is substantially the same as the thickness of a predetermined second single crystalline semiconductor layer.

16. The semiconductor device according to claim 12, wherein a MOS transistor is formed in a predetermined first single crystalline semiconductor layer of the first region; a bipolar transistor is formed in a predetermined second single crystalline semiconductor layer of the second region; the first and second single crystalline semiconductor layers have substantially the

same height from the surface of the semiconductor substrate; and the thickness of the semiconductor layer lower than the gate electrode of the MOS transistor is substantially the same as the thickness of a predetermined second single crystalline semiconductor layer.

17. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor substrate by laminating a buried insulating film, a single crystalline semiconductor layer, a first insulating film subsequently in this order;

etching the first insulating film and the single crystalline semiconductor layer to form a plurality of laminate films consisting of the single crystalline semiconductor layer and the first insulating film in the buried insulating film;

forming a second insulating film on the semiconductor substrate so as to cover the laminate films;

flattening the second insulating film until the height of the second insulating film from the semiconductor substrate becomes the same as that of the first insulating film, thereby forming an element isolation region;

etching away the first insulating film constituting at least one laminate film to expose a

surface of the single crystalline semiconductor layer under the first insulating film; and

depositing the single crystalline semiconductor to a predetermined depth on the exposed single crystalline semiconductor layer.

18. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor substrate by laminating a buried insulating film, a single crystalline semiconductor element, a first insulating film subsequently in this order;

etching the first insulating film and the single crystalline semiconductor layer to form a plurality of laminate films consisting of the single crystalline semiconductor layer and the first insulating film on the buried insulating film;

forming a second insulating film on the semiconductor substrate so as to cover the laminate films;

flattening the second insulating film until the height of the second insulating film becomes substantially the same as that of the first insulating film to form an element isolation region;

etching away at least one laminate film and simultaneously etching away the buried insulating film under the removed laminate film, thereby exposing a surface of the semiconductor substrate;

etching the first insulating film constituting at least one laminate film excluding the removed laminate film, thereby exposing a surface of the single crystalline semiconductor layer under the first insulating film; and

depositing a single crystalline semiconductor on the exposed single crystal semiconductor layer to thicken the single crystalline semiconductor layer, and simultaneously forming a single crystalline semiconductor layer on an exposed surface of the semiconductor substrate, thicker than the single crystalline semiconductor layer formed on the buried insulating film.

19. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor substrate by laminating a buried insulating film, a single crystalline semiconductor layer, a first insulating film subsequently in this order;

etching the first insulating film and the single crystalline semiconductor layer to form a plurality of laminate films consisting of the single crystalline semiconductor layer and the first insulating film on the buried insulating film;

forming a second insulating film on the semiconductor substrate so as to cover the laminate films;

flattening the second insulating film until the height of the second insulating film from the semiconductor surface becomes substantially the same as that of the first insulating film to form an element isolation region;

etching away the first insulating film constituting at least one laminate film to expose a surface of the single crystalline semiconductor layer under the first insulating film;

forming a MOS transistor on the single crystalline semiconductor layer whose surface is exposed;

etching away the first insulating film formed on a predetermined single crystalline semiconductor layer within the single crystalline semiconductor layer covered with the first insulating film;

depositing a single crystalline semiconductor on the single crystalline semiconductor layer having the MOS transistor formed therein and on the single crystal semiconductor layer whose surface is exposed; and

forming a bipolar transistor on a predetermined single crystalline semiconductor layer whose surface is exposed.

20. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor substrate by laminating a buried insulating film, a single crystalline semiconductor layer, and a first insulating film

subsequently;

etching the first insulating film and the single crystalline semiconductor layer to form a plurality of laminate films consisting of the single crystalline semiconductor layer and the first insulating film on the buried insulating film;

forming a second insulating film on the semiconductor substrate so as to cover the laminate films;

flattening the second insulating film until the height of the second insulating film from the semiconductor surface becomes substantially the same as that of the first insulating film to form an element isolation region;

etching away at least one laminate film and simultaneously etching away the buried insulating film under the removed laminate film to expose a surface of the underlying semiconductor substrate;

depositing the single crystalline semiconductor layer in contact with the surface of the exposed semiconductor substrate;

etching away the first insulating film constituting at least one laminate film excluding the removed laminate film to expose a surface of the single crystalline semiconductor surface;

forming a MOS transistor on the exposed single crystalline semiconductor layer;

depositing a single crystalline semiconductor on  
the single crystalline semiconductor layer having the  
MOS transistor formed therein and simultaneously  
depositing on the single crystal semiconductor layer  
5 formed on the semiconductor substrate whose surface is  
exposed, thereby rendering the height of the single  
crystalline semiconductor layer having the MOS  
transistor therein, from the surface of the  
semiconductor substrate, substantially the same as that  
10 of the single crystalline semiconductor layer formed on  
the semiconductor substrate whose surface is exposed;  
and

depositing the single crystalline semiconductor  
and forming a bipolar transistor on the single  
15 crystalline semiconductor layer formed on the  
semiconductor substrate whose surface is exposed.